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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/017,777	12/13/2001	Edward P. Kuzemchak	TI-32443	6142

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TEXAS INSTRUMENTS INCORPORATED
P O BOX 655474, M/S 3999
DALLAS, TX 75265

EXAMINER	
VO, TED T	

ART UNIT	PAPER NUMBER
2192	

DATE MAILED: 05/03/2005

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/017,777	KUZEMCHAK ET AL.	
	Examiner	Art Unit	
	Ted T. Vo	2192	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *29 November 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-16* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *4,5,7,9,11,12 and 14* is/are allowed.

6)☒ Claim(s) *1-3,6,8,10,13 and 15* is/are rejected.

7)☒ Claim(s) *16* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *11/29/04*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

1. This action is in response to the communications filed on 11/29/2004 responsive to the Office Action dated on 08/26/04.

Response to Amendment

2. The amendment filed on 11/29/04 has been considered in this application.

In view of the newly submitted Oath/Declaration on 01/21/05, the prior objection to this issue is withdrawn.

A certified copy of the priority document has been received on dated 01/21/05.

Claims 1, 4, 6, 7, 10, and 15-16 are amended.

Claims 1-3, 6, 8, 13, 10, 15-16,which are amended, necessitated the new ground(s) of rejection presented in this Office action, accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a).

Applicant's arguments with respect to claims 1-3, 6, 8, 13, 10, 15-16 have been considered but are moot in view of the new ground(s) of rejection. See Rationale in Claim Rejections.

Claims 1-16 are pending in this application.

Double Patenting

3. The nonstatutory double patenting rejection is based on a judicially created doctrine grounded in public policy (a policy reflected in the statute) so as to prevent the unjustified or improper timewise extension of the "right to exclude" granted by a patent and to prevent possible harassment by multiple assignees. See *In re Goodman*, 11 F.3d 1046, 29 USPQ2d 2010 (Fed. Cir. 1993); *In re Longi*, 759 F.2d 887, 225 USPQ 645 (Fed. Cir. 1985); *In re Van Ornum*, 686 F.2d 937, 214 USPQ 761 (CCPA 1982); *In re Vogel*, 422 F.2d 438, 164 USPQ 619 (CCPA 1970); and, *In re Thorington*, 418 F.2d 528, 163 USPQ 644 (CCPA 1969).

A timely filed terminal disclaimer in compliance with 37 CFR 1.321(c) may be used to overcome an actual or provisional rejection based on a nonstatutory double patenting ground

provided the conflicting application or patent is shown to be commonly owned with this application. See 37 CFR 1.130(b).

Effective January 1, 1994, a registered attorney or agent of record may sign a terminal disclaimer. A terminal disclaimer signed by the assignee must fully comply with 37 CFR 3.73(b).

Claim 10 is provisionally rejected under the judicially created doctrine of obviousness-type double patenting as being unpatentable over claim 1 of copending Application No. 10/022,972 which is cited on the amended specification filed on 11/29/04. Although the conflicting claims are not identical, they are not patentably distinct from each other because Claim 10 and Claim 1 of Application No. 10/022,972 all perform the similarly function.

This is a provisional obviousness-type double patenting rejection because the conflicting claims have not in fact been patented.

Claim Objections

4. Claim 16 is object to because the preamble of Claim 16 "A Digital system of Claim 15" is not in the same scope as set forth in Claim 15, "A digital software verification system". Amendment for clarifying the scope of the claim is required.

Claim Rejections - 35 USC § 102

5. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

6. Claims 1-3, 6, 8, 10, 13, 15 are rejected under 35 U.S.C. 102(b) as being anticipated by Guerra et al., "Cycle and Phase Accurate DSP Modeling and Integration for HW/SW Co-Verification", 1999-ACM.

Given the broadest reasonable interpretation of followed claims in light of the specification.

As per Claim 1:

The whole Guerra reference should be incorporated.

Guerra discloses simulation of a develop model against an accurate model. The teaching covers the limitations:

"*A method for verifying that two programs are equivalent, the method comprising the steps of:*

executing a first program at source hardware operating according to a first instruction set architecture (See page 964, right column, C/C++ based cycle-accurate ISA, or RTL models. See page 965, left column, first, second, and third columns, for example: processor model, "first program" which is simulated against co-verification model. See page 965, section 2.2 Model Structure or see page 966 section 2.3, "Arguments for a Cycle-Accurate 'Core Model');

collecting a first set of events that are created by the first program while it is being executed (Refer to Cycle/phase accurate fashion. See page 965, Model Structure, For example, "each executed instruction can trigger one or more software events...". Or, Figure 1, Figure 4, or see either see Figure 7 having instructions in the right and execution circle in the left)

executing a second program at target hardware operating according to a second instruction set architecture (See page 964, right column, C/C++ based cycle-accurate ISA, or RTL models. See page 965, left column, first, second and third columns, for example DSP co-verification model which is used as co-verifying against processor model. See page 966 section 2.3, "Arguments for a Cycle-Accurate 'Core Model' or page 965, section 2.2 Model Structure);

collecting a second set of events that are created by the second program while it is being executed (Refer to Cycle/phase accurate fashion. See page 965, Model Structure, For example, "each executed instruction can trigger one or more software events...". Or, Figure 1, Figure 4 Or, Figure 1, Figure 4, or see either see in Figure 7 having execution circle in the left and instructions in the right)

determining if the first set of events is equivalent to the second set of events by reconciling the first set of events and the second set of events; and indicating the first program is not equivalent to the second program if an unreconciled event is discovered during the step of determining" (Refer to co-simulation as disclosed by this reference, debugging, showing waveform and software debug of Figure 7).

As per Claim 2: Guerra discloses, "*The method of claim 1, wherein the step of determining comprises the steps of: matching each event of the first set of events to a corresponding event in the second set of events; declaring the existence of an unreconciled event if an event in the first set of events does not have a corresponding event in the second set of events; and declaring the existence of an unreconciled event if an event in the second set of events does not have a corresponding event in the first set of events.*" (See page 967, Figure 4 and page 968, section 3.4: Debugging, particularly referring to VHDL-Based system simulation, VHDL simulator).

As per Claim 3: Guerra discloses, "*The method of claim 2, wherein: the step of collecting a first set of events comprises developing a logical state for each event of the first set of events* (See Figure 1. See section 3, Integration HDL Environment. See page 967, Figure 4, "write to ISA model", See figure 7)*; the step of collecting a second set of events comprises developing a logical state for each event of the second set of events* (See Figure 1. See page 967, Figure 4, "write to ISA model", Figure 7)*; and the step of matching comprises comparing the logical state of each event of the first set of events to the logical state of the corresponding event in the second set of events*" (See section 3.4, Debugging and referring to "simulation").

As per Claim 6: Guerra discloses, "*The method of claim 1, wherein the step of indicating comprises activating a debugging capability in a software development system during the step of executing a first program at the point where the unreconciled event is discovered and activating the debugging capability in the software development system during the step of executing a second program at the point where the unreconciled event is discovered.*" (See page 968, Section 3.4 Debugging, particularly see Figure 6).

As per Claim 8: Guerra discloses, "*The method of claim 1, wherein: the steps of collecting a first set of events and collecting a second set of events comprise treating references to address*

registers in instructions as symbols; and the step of determining comprises computing the effective addresses of the analogous references in the first set of event and the second set of events when reconciling the first set of events and the second set of events." (See Figure 6, "Compiler"; where a compiler is capable to *treat references to address registers in instructions as symbols;* See page 966, section 2.3, "using instruction-accurate approach", "pipeline", "decode stage" etc., having the capability to *determine computing the effective addresses*).

As per Claim 13: Guerra discloses, "*The method of claim 1, wherein the means for executing, collecting, determining, and indicating is a first verification program whereby the verification program causes a first program to be executed by a first software development system, causes a second program to be executed by a second software development system, and receives information from the first software development system and the second software development system to perform the steps of collecting, determining, and indicating.*" (See page 968, section 3.4, and particularly, diagrams of Figures 6(a) and (b)).

As per Claim 10: Guerra discloses, "*A method of for verifying that two programs are equivalent, the method comprising the steps of:*

executing a first program;

collecting a first set of events that are created by the first program while it is being executed;

executing a second program;

collecting a second set of events that are created by the second program while it is being executed

determining if the first set of events is equivalent to the second set of events by reconciling the first set of events and the second set of events; and indicating the first program is not equivalent to the second program if an unreconciled event is discovered during the step of determining" (See rationale in Claim 1);

wherein the steps of collecting a first set of events and collecting a second set of events comprise:

determining that a first instruction is in the instruction pipeline; calculating the current effective address delay of the instruction in the pipeline (based on the broad recitation: see page 966, see right column, last paragraph, "5-stage pipeline", "branch prediction are example that might cause a delay" → "calculating"); *finding that a valid effective address for the instruction is available based on the current effective address delay of the instruction; computing the effective address of the first instruction if a valid effective address is not available; and reporting the effective address of the instruction.*" (See page 966, section 2.3, Figure 2, Figure 3).

As per Claim 15:

Regarding "A digital software verification system, comprising:
a general purpose computer;
a first microprocessor for executing application program;
first emulation hardware, coupled between the first microprocessor and the general purpose computer, for controlling the operation of the first microprocessor according to a first instruction set architecture;
a second microprocessor for executing application programs; and
second emulation hardware, coupled between the second microprocessor and
the general purpose computer, for controlling the operation of -the second microprocessor according to a second instruction set architecture" (Referring to the VHDL environment, as seen in Pages 964-965, Introduction, and Section 2, Processor Co-verification Model, and Figure 5);

Regarding "wherein the general purpose computer is programmed to perform a method for verifying that a target application program is equivalent to a source application program, the method comprising the steps of:
causing the first emulation hardware to execute a first program at the first microprocessor;
collecting a first set of events that are performed by the first program while it is being executed;
causing the second emulation hardware to execute a second program at the second microprocessor;

collecting a second set of events that are performed by the second program while it is being executed;

determining if the first set of events is equivalent to the second set of events; and indicating the first program is not equivalent to the second program if a mismatch is discovered during the step of determining" See rationale in Claim 1.

Allowable Subject Matter

7. Claims 4, 5, 7, 9, 11-12, 14 are allowed.

Claim 16 is objected to as above, and also objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

Claim 16 is allowable because its limitation is corresponding to the allow claim 4.

Conclusion

8. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

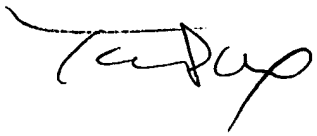
A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Ted T. Vo whose telephone number is (571) 272-3706. The examiner can normally be reached on 8:00AM to 5:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Tuan Q. Dam can be reached on (571) 272-3694. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Any inquiry of a general nature or relating to the status of this application should be directed to the TC 2100 Group receptionist: 571-272-2100. Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for

published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR System, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).



Ted T. Vo
Primary Examiner
Art Unit 2192
April 25, 2005